Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended): An interconnection system for a plurality of processing elements (PEs), each PE having a communications port for transmitting and receiving data and commands, each PE corresponding to a position of a matrix element where the position of the matrix element has at least a North, East, South, or West matrix position neighbor, a pair of matrix neighbors is mutually exclusive when one neighbor is either in the North or South direction relative to the position of the matrix element and the other neighbor is either in the East or West direction relative to the position, the interconnection system comprising:

a plurality of clusters of PEs, each cluster comprising a portion of the plurality of PEs~~inter-PE connection paths~~; and

a cluster switch connected to said PEs in each cluster, said portion of the plurality of PEs assigned so that each PE in said portion of the plurality of PEs has its mutually exclusive matrix position neighbors in at most two of the plurality of clusters of PEs, at least two PEs in one cluster sharing a connection to their common neighbor in another cluster when communicating to their mutually exclusive matrix position neighbors through the cluster switch~~so as to combine mutually exclusive inter-PE connection paths and to thereby substantially reduce the number of communications paths required to provide inter-PE connectivity equivalent to that of conventional torus-connected PE arrays~~.

2-43. (canceled)

44. (currently amended): An array processor comprising:

a plurality of processing elements(PEs), each PE corresponding to a position of a matrix element where the position of the matrix element has at least a North, East, South, or West matrix position neighbor, a pair of matrix neighbors is mutually exclusive when one neighbor is either in the North or South direction relative to the position of the matrix element and the other neighbor is either in the East or West direction relative to the position of the matrix element, the plurality of PEs arranged in a plurality of clusters, each cluster including a portion of the plurality of processing elements, the portion of the plurality of PEs selected so that each PE in said portion of the plurality of PEs has its mutually exclusive matrix position neighbors in at most two of the plurality of clusters, ~~which communicate in mutually exclusive torus directions with the processing elements of at least one other cluster~~; and

cluster switches connecting the plurality of clusters, ~~ed to the clusters to provide said mutually exclusive torus direction communication~~ at least two PEs in each cluster sharing a connection to their common neighbor to another cluster through the cluster switch.

45. (previously presented): The array processor of claim 44 wherein each cluster includes an equal number of processing elements.

46. (previously presented): The array processor of claim 44 wherein at least one cluster includes a torus transpose pair of processing elements.

47. (previously presented): The array processor of claim 44 wherein the cluster switches provide inter-PE connectivity equivalent to a torus connected array.

48. (previously presented): The array processor of claim 44 wherein the cluster switches provide direct communication between processing elements in a transpose processing element pair within a cluster.

49. (previously presented): The array processor of claim 44 wherein the clusters of processing elements are scaleable.

50. (previously presented): The array processor of claim 44 wherein the processing elements of each cluster are located in close physical proximity to each other.

51. (previously presented): The array processor of claim 44 further comprising a single instruction multiple data (SIMD) controller which broadcasts data to said plurality of processing elements.

52. (previously presented): The array processor of claim 51 wherein each processing element performs a calculation and transmits the results of the calculation to a nearest neighbor processing element.

53-56. (canceled)

57. (previously presented): The array processor of claim 44 wherein the clusters of processing elements correspond to slices of a torus array shifted and wrapped into a cylinder.

58. (previously presented): The array processor of claim 44 wherein each processing element (PE) is defined as $PE_{i,j}$, where i and j refer to the respective row and column PE positions within a conventional torus-connected array, and where i = 0,1,2, ... N-1 and j = 0, 1, 2, . . . N-1, said PEs arranged in clusters $PE_{(i+a)(ModN),(j+N-a)(ModN)}$, for any i,j and for all $a \in \{0,1,...,N-1\}$.

59. (previously presented): The array processor of claim 44 wherein each cluster switch multiplexes communications from processing elements within a cluster for transmission to another cluster.